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DATE: Wednesday, June 01, 2005

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☐ 1. Document ID: US 20050045206 A1

L3: Entry 1 of 6 File: PGPB Mar 3, 2005

PGPUB-DOCUMENT-NUMBER: 20050045206
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20050045206 A1

TITLE: Post-etch clean process for porous low dielectric constant materials

PUBLICATION-DATE: March 3, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Smith, Patricia Beauregard	Colleyville	TX	US	
Park, Heungsoo	McKinney	TX	US	
Zielinski, Eden	Richardson	TX	US	

US-CL-CURRENT: 134/16; 134/17, 134/19, 134/25.4

ABSTRACT:

Standard post-etch photoresist clean procedures for porous dielectric materials manufacturing may involve wet cleans in which a solvent is used for polymer residue removal. In many cases, the components of the solvent are absorbed into porous film layers and can later volatilize during subsequent metal deposition steps. A low pressure anneal of limited duration and high temperature, performed after the wet clean and prior to metal deposition, satisfactorily removes the absorbed components.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D

☐ 2. Document ID: US 20040002221 A1

L3: Entry 2 of 6 File: PGPB Jan 1, 2004

PGPUB-DOCUMENT-NUMBER: 20040002221
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040002221 A1

TITLE: Productivity enhancing thermal sprayed yttria-containing coating for plasma reactor

PUBLICATION-DATE: January 1, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
O'Donnell, Robert J.	Fremont	CA	US	
Daugherty, John E.	Newark	CA	US	

US-CL-CURRENT: 438/710

ABSTRACT:

Components of semiconductor processing apparatus comprise thermal sprayed yttria-containing coatings that provide erosion, corrosion and/or corrosion-erosion resistance in plasma atmospheres. The coatings can protect substrates from physical and/or chemical attack.

☐ 3. Document ID: US 20030194877 A1

L3: Entry 3 of 6 File: PGPB Oct 16, 2003

PGPUB-DOCUMENT-NUMBER: 20030194877
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030194877 A1

TITLE: Integrated etch, rinse and dry, and anneal method and system

PUBLICATION-DATE: October 16, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Yau, Wai-Fan	Los Altos	CA	US	
Fairbairn, Kevin P.	Los Gatos	CA	US	
Barnes, Michael	San Ramon	CA	US	

US-CL-CURRENT: 438/745

ABSTRACT:

A method is provided processing workpieces including etching metal from a workpiece to define metal structures on the workpiece and transporting the workpiece through a controlled environment passage between an etch chamber and a wet clean module after the etching. A wet cleaning and drying of the workpiece is performed in the wet clean module to remove metal etch residues from the workpiece. The workpiece is transported through the controlled environment passage to an annealing chamber after wet cleaning. An annealing is performed and the metal structures are capped before exposing the workpiece to ambient atmosphere after etching, wet cleaning, and annealing. The capping may be performed in situ with the annealing in a CVD chamber. The metal etch process may include performing a timed etch for etching back a portion of a metal layer followed by a slow to endpoint etch with an endpoint signal, followed by a timed over etch. The workpiece is transferred from

the etch chamber to the wet clean module for the wet cleaning after the such a process while maintaining a non-oxidizing atmosphere surrounding the workpiece so as to inhibit corrosion of the metal structures prior to the wet cleaning of the workpiece. The timed etch, the slow to endpoint etch, and the timed over etch is performed in three separate chambers. Or, the timed etch is performed in a first etch chamber and the slow to endpoint etch and the timed over etch are performed in a second etch chamber.

☐ 4. Document ID: US 20030045131 A1

L3: Entry 4 of 6 File: PGPB Mar 6, 2003

PGPUB-DOCUMENT-NUMBER: 20030045131
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030045131 A1

TITLE: Method and apparatus for processing a wafer

PUBLICATION-DATE: March 6, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Verbeke, Steven Verha	San Francisco	CA	US	
Truman, J. Kelly	Morgan Hill	CA	US	
Lane, Christopher T.	San Jose	CA	US	
Somekh, Sasson R.	Los Altos Hills	CA	US	

US-CL-CURRENT: 438/795

ABSTRACT:

A method of a single wafer wet/dry cleaning apparatus comprising:

a transfer chamber having a wafer handler contained therein;

a first single wafer wet cleaning chamber directly coupled to the transfer chamber; and

a first single wafer ashing chamber directly coupled to the transfer chamber.

☐ 5. Document ID: US 20030045098 A1

L3: Entry 5 of 6 File: PGPB Mar 6, 2003

PGPUB-DOCUMENT-NUMBER: 20030045098
PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030045098 A1

TITLE: Method and apparatus for processing a wafer

PUBLICATION-DATE: March 6, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Verhaverbeke, Steven	San Francisco	CA	US	
Truman, J. Kelly	Morgan Hill	CA	US	
Lane, Christopher T.	San Jose	CA	US	

US-CL-CURRENT: 438/689; 118/50.1, 134/1, 134/1.3, 204/193, 430/329

ABSTRACT:

A method of a single wafer wet/dry cleaning apparatus comprising:

a transfer chamber having a wafer handler contained therein;

a first single wafer wet cleaning chamber directly coupled to the transfer chamber; and

a first single wafer ashing chamber directly coupled to the transfer chamber.

☐ 6. Document ID: JP 2005072601 A, US 20050045206 A1

L3: Entry 6 of 6 File: DWPI Mar 17, 2005

DERWENT-ACC-NO: 2005-221200
DERWENT-WEEK: 200523

TITLE: Semiconductor wafer cleaning method, involves cleaning polymer residue from etched wafer using wet clean solvent, and lower pressure annealing etched wafer to remove component of solvent prior to metal deposition

INVENTOR: PARK, H; SMITH, P B ; ZIELINSKI, E

PRIORITY-DATA: 2003US-0647985 (August 26, 2003)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 2005072601 A	March 17, 2005		007	H01L021/304
US 20050045206 A1	March 3, 2005		005	B08B003/04

INT-CL (IPC): B08 B 3/04; H01 L 21/304; H01 L 21/768

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
ANNEAL$	0
ANNEAL	65977
ANNEALA	2
ANNEALABFLITY	1
ANNEALABIE	1
ANNEALABILITY	26
ANNEALABLE	175
ANNEALABLEWHITE	1
ANNEALAD	1
ANNEALAGE	1
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L2: Entry 9 of 22 File: PGPB Oct 16, 2003

PGPUB-DOCUMENT-NUMBER: 20030194877
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030194877 A1

TITLE: Integrated etch, rinse and dry, and anneal method and system

PUBLICATION-DATE: October 16, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Yau, Wai-Fan	Los Altos	CA	US	
Fairbairn, Kevin P.	Los Gatos	CA	US	
Barnes, Michael	San Ramon	CA	US	

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	COUNTRY	TYPE CODE
Applied Materials, Inc.				02

APPL-NO: 10/ 124437 [PALM]
DATE FILED: April 16, 2002

INT-CL: [07] H01 L 21/302, H01 L 21/461

US-CL-PUBLISHED: 438/745
US-CL-CURRENT: 438/745

REPRESENTATIVE-FIGURES: 1

ABSTRACT:

A method is provided processing workpieces including etching metal from a workpiece to define metal structures on the workpiece and transporting the workpiece through a controlled environment passage between an etch chamber and a wet clean module after the etching. A wet cleaning and drying of the workpiece is performed in the wet clean module to remove metal etch residues from the workpiece. The workpiece is transported through the controlled environment passage to an annealing chamber after wet cleaning. An annealing is performed and the metal structures are capped before exposing the workpiece to ambient atmosphere after etching, wet cleaning, and annealing. The capping may be performed in situ with the annealing in a CVD chamber. The metal etch process may include performing a timed etch for etching back a portion of a metal layer followed by a slow to endpoint etch with an endpoint signal, followed by a timed over etch. The workpiece is transferred from the etch chamber to the wet clean module for the wet cleaning after the such a process while maintaining a non-oxidizing atmosphere surrounding the workpiece so as to inhibit corrosion of the metal structures prior to the wet cleaning of the workpiece. The timed etch, the slow to endpoint etch, and the timed over etch is

performed in three separate chambers. Or, the timed etch is performed in a first etch chamber and the slow to endpoint etch and the timed over etch are performed in a second etch chamber.

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Search Results - Record(s) 11 through 20 of 22 returned.

☐ 11. Document ID: US 20030045131 A1

L2: Entry 11 of 22 File: PGPB Mar 6, 2003

PGPUB-DOCUMENT-NUMBER: 20030045131
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030045131 A1

TITLE: Method and apparatus for processing a wafer

PUBLICATION-DATE: March 6, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Verbeke, Steven Verha	San Francisco	CA	US	
Truman, J. Kelly	Morgan Hill	CA	US	
Lane, Christopher T.	San Jose	CA	US	
Somekh, Sasson R.	Los Altos Hills	CA	US	

US-CL-CURRENT: 438/795

ABSTRACT:

A method of a single wafer wet/dry cleaning apparatus comprising:

a transfer chamber having a wafer handler contained therein;

a first single wafer wet cleaning chamber directly coupled to the transfer chamber; and

a first single wafer ashing chamber directly coupled to the transfer chamber.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 12. Document ID: US 20030045098 A1

L2: Entry 12 of 22 File: PGPB Mar 6, 2003

PGPUB-DOCUMENT-NUMBER: 20030045098
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030045098 A1

TITLE: Method and apparatus for processing a wafer

PUBLICATION-DATE: March 6, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Verhaverbeke, Steven	San Francisco	CA	US	
Truman, J. Kelly	Morgan Hill	CA	US	
Lane, Christopher T.	San Jose	CA	US	

US-CL-CURRENT: 438/689; 118/50.1, 134/1, 134/1.3, 204/193, 430/329

ABSTRACT:

A method of a single wafer wet/dry cleaning apparatus comprising:

a transfer chamber having a wafer handler contained therein;

a first single wafer wet cleaning chamber directly coupled to the transfer chamber; and

a first single wafer ashing chamber directly coupled to the transfer chamber.

☐ 13. Document ID: US 6858361 B2

L2: Entry 13 of 22 File: USPT Feb 22, 2005

US-PAT-NO: 6858361
DOCUMENT-IDENTIFIER: US 6858361 B2

TITLE: Methodology for repeatable post etch CD in a production tool

DATE-ISSUED: February 22, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mui; David S. L.	Fremont	CA	94539	
Sasano; Hiroki	Sunnyvale	CA	94085	
Liu; Wei	San Jose	CA	95129	

US-CL-CURRENT: 430/30; 156/345.24, 257/E21.525, 355/40, 355/55, 356/625, 356/636, 430/313, 438/16, 438/7, 438/8

ABSTRACT:

A method and apparatus for processing a semiconductor wafer is provided for reducing dimensional variation by feeding forward information relating to photoresist mask CD and profile to adjust the next process the inspected wafer will undergo (e.g., a photoresist trim process). After the processing step, dimensions

of a structure formed by the process, such as the CD of a gate formed by the process, are measured, and this information is fed back to the process tool to adjust the process for the next wafer to further reduce dimensional variation. By taking into account photoresist CD and profile variation when choosing a resist trim recipe, post-etch CD is decoupled from pre-etch CD and profile. With automatic compensation for pre-etch CD, a very tight distribution of post-etch CD is achieved. In certain embodiments, the CD and profile measurements, trim, etch processing and post-etch cleaning are performed at a single module in a controlled environment. All of the transfer and processing steps performed by the module are performed in a clean environment, thereby increasing yield by avoiding exposing the wafer to the atmosphere and possible contamination between steps.

33 Claims, 15 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 14

☐ 14. Document ID: US 6800142 B1

L2: Entry 14 of 22 File: USPT Oct 5, 2004

US-PAT-NO: 6800142
DOCUMENT-IDENTIFIER: US 6800142 B1

TITLE: Method for removing photoresist and post-etch residue using activated peroxide followed by supercritical fluid treatment

DATE-ISSUED: October 5, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Tipton; Adrianne Kay	Fremont	CA		
Shrinivasan; Krishnan	San Jose	CA		
Banerjee; Souvik	Fremont	CA		
Humayun; Raashina	Fremont	CA		
Joyce; Patrick Christopher	San Jose	CA		

US-CL-CURRENT: 134/26; 134/1, 134/1.3, 134/19, 134/2, 134/28, 134/29, 134/30, 134/34, 257/E21.255, 438/906

ABSTRACT:

Methods for cleaning semiconductor wafers are presented. Contaminants, particularly photoresist and post-etch residue, are removed from semiconductor wafers. A wafer or wafers is first treated with a peroxide-containing medium, for example, to oxidatively cleave bond structures of contaminants on the wafer work surface. Excitation energy is used to activate the peroxide-containing medium toward the formation of radical species. After treatment with the peroxide-containing medium, a supercritical fluid treatment is used to remove any remaining contaminants as well as to condition the wafer for subsequent processing.

46 Claims, 4 Drawing figures

Exemplary Claim Number: 1
Number of Drawing Sheets: 3

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Ds

☐ 15. Document ID: US 6624127 B1

L2: Entry 15 of 22 File: USPT Sep 23, 2003

US-PAT-NO: 6624127
DOCUMENT-IDENTIFIER: US 6624127 B1

TITLE: Highly polar cleans for removal of residues from semiconductor structures

DATE-ISSUED: September 23, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Brask; Justin K.	Portland	OR		
Turkot, Jr.; Robert B.	Hillsboro	OR		
Ramachandrarao; Vijayakumar S.	Hillsboro	OR		

US-CL-CURRENT: 510/175; 134/2, 134/3, 510/176, 510/177

ABSTRACT:

Supercritical carbon dioxide may be utilized to remove resistant residues such as those residues left when etching dielectrics in fluorine-based plasma gases. The Supercritical carbon dioxide may include an ionic liquid in one embodiment.

10 Claims, 0 Drawing figures
Exemplary Claim Number: 1

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Ds

☐ 16. Document ID: US 6620743 B2

L2: Entry 16 of 22 File: USPT Sep 16, 2003

US-PAT-NO: 6620743
DOCUMENT-IDENTIFIER: US 6620743 B2

TITLE: Stable, oxide-free silicon surface preparation

DATE-ISSUED: September 16, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Pagliaro, Jr.; Robert H.	Penarth			GB

Doty; Mitchell L.	Higley	AZ
King; Diane M.	Cave Creek	AZ

US-CL-CURRENT: 438/787; 134/2, 134/3, 257/E21.228, 438/753, 438/906

ABSTRACT:

Methods are provided for producing a hydrogen-terminated silicon wafer surface with high stability against oxidation. The silicon wafer is cleaned with ammonium hydroxide/hydrogen peroxide/water, etched with high purity, heated dilute hydrofluoric acid, rinsed in-situ with ultrapure water at room temperature, and is spin-dried with heat ionized purge gas. The stability of the surface of the silicon wafer is assured by optimizing to minimize particle addition at each step. The silicon wafer produced by the method is stable in a normal clean room environment for greater than 3 days and has been demonstrated to last without significant oxide regrowth for greater than 7 days.

32 Claims, 10 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 8

☐ 17. Document ID: US 6596635 B1

L2: Entry 17 of 22 File: USPT Jul 22, 2003

US-PAT-NO: 6596635
DOCUMENT-IDENTIFIER: US 6596635 B1

TITLE: Method for metallization of a semiconductor substrate

DATE-ISSUED: July 22, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Tiku; Shiban K.	Camarillo	CA		
Knoedler; Heather L.	Thousand Oaks	CA		
Burton; Richard S.	Thousand Oaks	CA		

US-CL-CURRENT: 438/674

ABSTRACT:

According to one embodiment, an NiV adhesion layer is deposited over the backside surface of a semiconductor substrate. The semiconductor substrate might comprise a group III-V compound semiconductor. The NiV adhesion layer can be deposited over the backside surface of the semiconductor substrate in, for example, a magnetron deposition system. In certain embodiments, the backside surface of the semiconductor surface may be cleaned to remove oxides from the surface prior to deposition of the NiV adhesion layer. After the NiV adhesion layer has been deposited, a gold seed layer is deposited over the NiV adhesion layer. Following deposition of the gold seed layer, a second gold layer is electroplated, or

otherwise deposited, over the gold seed layer. In one embodiment, the invention is a structure fabricated according to the process steps described above.

23 Claims, 4 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 4

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 18. Document ID: US 6277762 B1

L2: Entry 18 of 22 File: USPT Aug 21, 2001

US-PAT-NO: 6277762
DOCUMENT-IDENTIFIER: US 6277762 B1

TITLE: Method for removing redeposited veils from etched platinum

DATE-ISSUED: August 21, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hwang; Jeng H.	Cupertino	CA		

US-CL-CURRENT: 438/714; 257/E21.311, 438/720, 438/734

ABSTRACT:

A method of etching a platinum electrode layer disposed on a substrate. The method comprises providing a substrate supporting a platinum electrode layer, an insulation layer on the platinum electrode layer, and a resist layer on the insulation layer. A portion of the insulation layer is etched by employing a plasma of an etchant gas to break through and to remove the portion of the insulation layer from the platinum electrode layer to expose part of the platinum electrode layer. The exposed part of the platinum electrode layer is then etched by employing a plasma of an etchant gas comprising argon. The etched platinum electrode layer is subsequently overetched by employing a high density plasma of an etchant gas to remove redeposited veils from the etched platinum electrode layer. The etched platinum electrode layer is employed in a semiconductor device.

83 Claims, 26 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 17

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 19. Document ID: US 6239038 B1

L2: Entry 19 of 22 File: USPT May 29, 2001

US-PAT-NO: 6239038

DOCUMENT-IDENTIFIER: US 6239038 B1
**** See image for Certificate of Correction ****

TITLE: Method for chemical processing semiconductor wafers

DATE-ISSUED: May 29, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Wen; Ziying	Gresham	OR	97030	

US-CL-CURRENT: 438/745

ABSTRACT:

A method and apparatus for processing semiconductor wafer blanks comprises an enclosed chamber with upper and lower plates with a plurality of fluid openings leading from a source of chemical cleaning fluids, flushing fluid and dry nitrogen gas. The top plate also acts as a vacuum chuck to hold the wafer after the top surface has been cleaned and may rotate or oscillate to enhance the cleaning of the lower wafer surface. The method includes a chemical cleaning of the wafer top followed by processing the lower surface by pumping appropriate chemicals through the lower plate center toward the wafer periphery while the wafer is extremely close to the surface so that the outward moving fluids cover the wafer surface and are sparingly used. As the chemicals flow toward the periphery, their strength is renewed by the addition of new chemicals pumped through additional holes.

20 Claims, 25 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 15

☐ 20. Document ID: US 6087265 A

L2: Entry 20 of 22 File: USPT Jul 11, 2000

US-PAT-NO: 6087265
DOCUMENT-IDENTIFIER: US 6087265 A

TITLE: Method for removing redeposited veils from etched platinum

DATE-ISSUED: July 11, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hwang; Jeng H.	Cupertino	CA		

US-CL-CURRENT: 438/706; 257/E21.311, 438/714, 438/720

ABSTRACT:

A method of etching a platinum electrode layer disposed on a substrate. The method

comprises providing a substrate supporting a platinum electrode layer, an insulation layer on the platinum electrode layer, and a resist layer on the insulation layer. A portion of the insulation layer is etched by employing a plasma of an etchant gas to break through and to remove the portion of the insulation layer from the platinum electrode layer to expose part of the platinum electrode layer. The exposed part of the platinum electrode layer is then etched by employing a plasma of an etchant gas comprising argon. The etched platinum electrode layer is subsequently overetched by employing a high density plasma of an etchant gas to remove redeposited veils from the etched platinum electrode layer. The etched platinum electrode layer is employed in a semiconductor device.

76 Claims, 26 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 17

Term	Documents
WET	548741
WETS	16230
CLEAN	644110
CLEANS	35930
(1 AND (WET ADJ CLEAN)).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	22
(L1 AND (WET CLEAN)).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	22

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Search Results - Record(s) 21 through 22 of 22 returned.

☐ 21. Document ID: US 6037264 A

L2: Entry 21 of 22 File: USPT Mar 14, 2000

US-PAT-NO: 6037264
DOCUMENT-IDENTIFIER: US 6037264 A

TITLE: Method for removing redeposited veils from etched platinum

DATE-ISSUED: March 14, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hwang; Jeng H.	Cupertino	CA		

US-CL-CURRENT: 438/714; 257/E21.311, 438/720, 438/734

ABSTRACT:

A method of etching a platinum electrode layer disposed on a substrate. The method comprises providing a substrate supporting a platinum electrode layer, an insulation layer on the platinum electrode layer, and a resist layer on the insulation layer. A portion of the insulation layer is etched by employing a plasma of an etchant gas to break through and to remove the portion of the insulation layer from the platinum electrode layer to expose part of the platinum electrode layer. The exposed part of the platinum electrode layer is then etched by employing a plasma of an etchant gas comprising argon. The etched platinum electrode layer is subsequently overetched by employing a high density plasma of an etchant gas to remove redeposited veils from the etched platinum electrode layer. The etched platinum electrode layer is employed in a semiconductor device.

54 Claims, 26 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 17

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 22. Document ID: JP 2005072601 A, US 20050045206 A1

L2: Entry 22 of 22 File: DWPI Mar 17, 2005

DERWENT-ACC-NO: 2005-221200
DERWENT-WEEK: 200523

TITLE: Semiconductor wafer cleaning method, involves cleaning polymer residue from etched wafer using wet clean solvent, and lower pressure annealing etched wafer to remove component of solvent prior to metal deposition

INVENTOR: PARK, H; SMITH, P B ; ZIELINSKI, E

PRIORITY-DATA: 2003US-0647985 (August 26, 2003)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 2005072601 A	March 17, 2005		007	H01L021/304
US 20050045206 A1	March 3, 2005		005	B08B003/04

INT-CL (IPC): B08 B 3/04; H01 L 21/304; H01 L 21/768

Term	Documents
WET	548741
WETS	16230
CLEAN	644110
CLEANS	35930
(1 AND (WET ADJ CLEAN)).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	22
(L1 AND (WET CLEAN)).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	22

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☐ 1. Document ID: US 20050045206 A1

L5: Entry 1 of 2 File: PGPB Mar 3, 2005

PGPUB-DOCUMENT-NUMBER: 20050045206
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20050045206 A1

TITLE: Post-etch clean process for porous low dielectric constant materials

PUBLICATION-DATE: March 3, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Smith, Patricia Beauregard	Colleyville	TX	US	
Park, Heungsoo	McKinney	TX	US	
Zielinski, Eden	Richardson	TX	US	

US-CL-CURRENT: 134/16; 134/17, 134/19, 134/25.4

ABSTRACT:

Standard post-etch photoresist clean procedures for porous dielectric materials manufacturing may involve wet cleans in which a solvent is used for polymer residue removal. In many cases, the components of the solvent are absorbed into porous film layers and can later volatilize during subsequent metal deposition steps. A low pressure anneal of limited duration and high temperature, performed after the wet clean and prior to metal deposition, satisfactorily removes the absorbed components.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: JP 2005072601 A, US 20050045206 A1

L5: Entry 2 of 2 File: DWPI Mar 17, 2005

DERWENT-ACC-NO: 2005-221200
DERWENT-WEEK: 200523

TITLE: Semiconductor wafer cleaning method, involves cleaning polymer residue from etched wafer using wet clean solvent, and lower pressure annealing etched wafer to remove component of solvent prior to metal deposition

INVENTOR: PARK, H; SMITH, P B ; ZIELINSKI, E

PRIORITY-DATA: 2003US-0647985 (August 26, 2003)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 2005072601 A	March 17, 2005		007	H01L021/304
US 20050045206 A1	March 3, 2005		005	B08B003/04

INT-CL (IPC): B08 B 3/04; H01 L 21/304; H01 L 21/768

Term	Documents
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ANNEALS	8708
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